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AMENDMENTS TO THE CLAIMS

1. **(Currently Amended)** A drive device for writing data transmitted by a host device onto a memory card in accordance with a command issued by the host device, the drive device comprising:

a receiving unit operable to receive a plurality of commands issued by the host device;

a writing unit operable, if a write end address of one of the received commands is consecutive with a write start address of a following command, to perform the data writing to the memory card by the consecutive commands in a single process; and

an analysis unit operable to decode the write-start address and a sector number of each command, the sector number being the number of sectors of data for writing with the command, wherein

the process involves processing to sequentially write data received from the host device to the memory card being repeated until a STOP instruction is given,

the process is activated when the analysis unit decodes a write-start address A and a sector number s from the one command, and involves the data writing being started from the write-start address A , and

a wait flag is appended to a command received from the host device.

the analysis unit analyzes the following command until the written sector number reaches s , and

if the command with the wait flag is received and a following command has yet to be received, the analysis unit waits for the following command to be received.

2. **(Previously Presented)** The drive device of claim 1, further comprising:
an instruction unit operable to give the STOP instruction at a point when a written sector number reaches $s + t$, where s is the sector number of the one command and t is the sector number of the following command.

3. **(Previously Presented)** The drive device of claim 2, wherein
the instruction unit gives the STOP instruction when the written sector number reaches $s + t$, if a write-start address B of the following command is consecutive with a write-end address $A + s$ of the one command.

4. **(Original)** The drive device of claim 3, wherein
the analysis unit judges whether a prohibit flag is appended to the following command, and
the instruction unit (i) gives the STOP instruction at a point when the written sector number reaches s if the prohibit flag is appended to the following command, and (ii) gives the STOP instruction at the point when the written sector number reaches $s + t$ if the prohibit flag is not appended to the following command and the write-start address B of the following command is consecutive with the write-end address $A + s$ of the one command.

5. **(Original)** The drive device of claim 3, wherein
the analysis unit judges whether a prohibit flag is appended to the one command, and

the instruction unit (i) gives the STOP instruction at a point when the written sector number reaches s , if the prohibit flag is appended to the one command, and (ii) gives the STOP instruction at the point when the written sector number reaches $s + t$, if the prohibit flag is not appended to the one command and the write-start address B of the following command is consecutive with the write-end address $A + s$ of the previous command.

6. (Cancelled)

7. (Previously Presented) The drive device in claim 1, wherein the host device transmits commands with a tag attached thereto to the drive device sequentially, the tags showing an order of the commands.

8. (Previously Presented) The drive device in claim 3, further comprising:
a storage unit operable to store commands received from the host device; and
a rearranging unit operable to rearrange the stored commands in order of the write-start addresses, wherein

the analysis unit performs the analysis in the rearranged order of the commands.

9. (Original) The drive device of claim 2, wherein
the analysis unit judges whether $s + t$ is an integer multiple of the number of sectors in an erasable block of the memory card, and

if judged in the negative, the instruction unit continues the process by not giving the STOP instruction even if the written sector number reaches $s + t$, and waits for a further command to be received.

10. (Currently Amended) A computer program for causing a computer to execute processing to write data transmitted by a host device onto a memory card in accordance with a command issued by the host device, the computer program being stored on a computer-readable medium and comprising code operable to cause the computer to perform the steps of:

receiving a plurality of commands issued by the host device;

if a write end address of one of the received commands is consecutive with a write start address of a following command, performing the data writing to the memory card by the consecutive commands in a single process; and

decoding, by an analysis unit, the write-start address and a sector number of each command, the sector number being the number of sectors of data for writing with the command, wherein

the process involves processing to sequentially write data received from the host device to the memory card being repeated until a STOP instruction is given,

the process is activated when a write-start address A and a sector number s from the one command is decoded, and involves the data writing being started from the write-start address A , and

a wait flag is appended to a command received from the host device.

the following command is analyzed until the written sector number reaches s and if the command with the wait flag is received and a following command has yet to be received, the analysis unit waits for the following command.

11. (Previously Presented) The computer program of claim 10, further comprising code operable to cause the computer to perform the step of:

giving the STOP instruction at a point when a written sector number reaches $s + t$, where s is the sector number of the one command and t is the sector number of the following command.

12. (Previously Presented) The computer program of claim 11, wherein the STOP instruction is given when the written sector number reaches $s + t$, if a write-start address B of the following command is consecutive with a write-end address $A + s$ of the one command.